REMARKS

The Examiner has rejected Claims 1-18 and 20-34 under 35 U.S.C. 103(a) as being unpatentable over Baldwin, U.S. Patent 5,764,228, in view of Chan et al., U.S. Patent 6,163,837, Brethour et al., U.S. Patent 6,577,316, and Huff et al., U.S. Patent 6,288,723. Applicant respectfully disagrees with such rejections.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir.1991).

With respect to the first element of the *prima facie* case of obviousness, the Examiner argues that it would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Huff, Brethour and Chan into the programmable pipeline graphics processing of Baldwin in order to achieve high speed, and increase pipeline processing throughput during execution of the instructions.

Applicant respectfully disagrees with this assertion, especially in view of the vast evidence to the contrary. In particular, applicant emphasizes that, while applicant claims a technique for programmable pixel processing, Brethour relates to programmable vertex processing and Huff relates to graphics card format conversion. Pixel processing relates to the problem of processing pixel-related elements in the graphics pipeline, while vertex processing relates to the processing of vertex data, a very different type of graphics-related data processed at a different point in a graphics pipeline. Moreover, graphics card format conversion relates to the problem of converting the format of graphics data for various graphics processors.

"In order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned." See MPEP 2141.01(a). To simply glean features from the arts of programmable vertex processing and graphics card format conversion and combine the same with the non-analogous art of programmable pixel processing would be improper and frustrate the inventive concepts of applicant, especially in view of the fundamentally different problems which the various arts address.

Thus, with respect to each of the independent claims, applicant respectfully asserts that at least the first element of the *prima facie* case of obviousness has not been met, in view of the foregoing evidence that it would not be obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Huff and Brethour with the art of programmable pixel processing.

To further emphasize the distinctions between applicant's claimed invention and the prior art of record, applicant has amended Claims 22 – 34, so as to incorporate the subject matter of Claim 9 and elaborate upon the claimed instruction set.

With respect to the third element of the *prima facie* case of obviousness, the Examiner has relied on various vertex processing-related instructions to make a prior art showing of applicant's claimed programmable pixel processing instruction set. To further emphasize the distinction between what applicant is claiming in Claims 22 - 34 and the art relied upon by the Examiner, applicant now claims that the instructions include "pixel data-related instructions" (emphasis added). Only applicant teaches and claims such a unique instruction set that is pixel data-related, and is specifically designed for programmable pixel processing.

Applicant asserts that the Examiner's proposed combination is significantly deficient in this regard. Just by way of example, the Examiner has relied on Claim 3 below from Baldwin to make a prior art showing of applicant's claimed "pixel data-related instructions include[ing] a no operation instruction."

"3. The method of claim 1, wherein no operations are performed on a primitive which is not located in any displayed window section." (Claim 3)

Such mention of "no operations," however, relates to primitive processing (i.e. vertex processing), and is not pixel-related, as claimed by applicant. Moreover, applicant notes that there is no mention of a no operation, in the specific context of a "no operation instruction" (emphasis added) that is a component of a "pixel-related instruction set."

Still yet, the Examiner has relied on the following excerpt from Baldwin to meet applicant's claimed "wherein the pixel data is swizzled."

"{GLINT as a Register File

The simplest way to view the interface to GLINT is as a flat block of memory-mapped registers (i.e. a register file). This register file appears as part of Region 0 of the PCI address map for GLINT. See the GLINT Hardware Reference Manual for details of this address map.

When a GLINT host software driver is initialized it can map the register file into its address space. Each register has an associated address tag, giving its offset from the base of the register file (since all registers reside on a 64-bit boundary, the tag offset is measured in multiples of 8 bytes). The most straightforward way to load a value into a register is to write the data to its mapped address. In reality the chip interface comprises a 16 entry deep FIFO, and each write to a register causes the written value and the register's address tag to be written as a new entry in the FIFO.

Programming GLINT to draw a primitive consists of writing initial values to the appropriate registers followed by a write to a command register. The last write triggers the start of rendering.

GLINT has approximately 200 registers. All registers are 32 bits wide and should be 32-bit addressed. Many registers are split into bit fields, and it should be noted that bit 0 is the least significant bit." (col. 13, lines 37-60)

Such excerpt, however, makes no disclosure, teaching or even suggestion of any sort of "swizzling," let alone swizzling of pixel data, as claimed by applicant. Despite this clear distinction, applicant has further distinguished this claimed feature by emphasizing, in Claims 22 – 34, that the swizzling includes a pixel-related vector component re-mapping, in order to expedite the prosecution of such claims.

Applicant thus respectfully asserts that at least the third element of the *prima facie* case of obviousness has not been met with respect to at least Claims 22 - 34, since the Examiner's cited excerpts do not disclose, teach or suggest applicant's claim language, as set forth hereinabove.

It appears that the Examiner has merely gleaned similar words from the various non-analogous references in an effort to show applicant's specifically claimed instruction set in the prior art. Applicant contends that such gleaning is improper, particularly because the various passages in such references do not relate to specific "pixel data-related instructions" that are components of a predetermined "instruction set" that may be used to take advantage of advanced features in a graphics hardware environment. Simply nowhere in the prior art is there disclosed, taught or suggested any sort of "pixel data-related instructions that include a no operation instruction, move instruction, multiply instruction, addition instruction, multiply and addition instruction, reciprocal instruction, reciprocal square root instruction, three component dot product instruction, four component dot product instruction, minimum instruction, maximum instruction, fraction instruction, exponential base two (2) instruction, logarithm base two (2) instruction, set on less than instruction for setting a destination to a predetermined number if a first source is less than a second source, set on greater or equal than instruction for setting a destination to a predetermined number if a first source is greater or equal than a second source, and kill pixel instruction" "wherein the pixel data is swizzled, and the swizzling includes a pixel-related vector component re-mapping."

With respect to Claims 10-18, it appears that the Examiner is invoking Official Notice, in that there has been no showing of such claimed features in the prior art. In response, applicant emphasizes that such claimed features are particularly beneficial when taken in combination with the remaining claim elements. Thus, applicant respectfully requests a specific prior art showing of ALL of the claim limitations, in combination with the remaining claim elements, or a notice of allowance. See excerpt from MPEP below:

> "If the applicant traverses such an [Official Notice] assertion the examiner should cite a reference in support of his or her position." See MPEP 2144.03.

All of the independent claims are thus deemed allowable along with any claims depending therefrom. An allowance or a specific prior art showing of applicant's claimed features is respectfully requested.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 505-5100. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 50-1351 (Order No. NVIDP036).

Respectfully submitted,

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